The documentation and process conversion measures necessary to comply with this revision shall be completed by 14 June 2016.

INCH-POUND

MIL-PRF-19500/765B

14 March 2016

SUPERSEDING

MIL-PRF-19500/765A

18 March 2013

## PERFORMANCE SPECIFICATION SHEET

SEMICONDUCTOR DEVICE, DIODE, SILICON, DUAL SCHOTTKY, COMMON CATHODE, ENCAPSULATED (THROUGH-HOLE AND SURFACE MOUNT), TYPE 1N7072, AND 1N7078

JAN, JANTX, JANTXV, AND JANS

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and MIL-PRF-19500.

## 1. SCOPE

- \* 1.1 <u>Scope</u>. This specification covers the performance requirements for a silicon, dual Schottky, center-tap power rectifier diode for use in high frequency switching power supplies and resonant power converters. Four levels of product assurance (JAN, JANTXV, and JANS) are provided for each encapsulated device.
- \* 1.2 <u>Package outlines</u>. The device package outlines are as follows: U3 in accordance with figure 1 and T3 (TO-257AA) in accordance with figure 2 for all encapsulated device types.
  - 1.3 Maximum ratings. Unless otherwise specified,  $T_A = +25$ °C.

Column 1	Column 2	Column 3	Column 4	Colu	mn 5	Column 6
Types	$V_{RWM}$	I <sub>O</sub> (1) (2)	$I_{FSM}$ (3) $t_p = 8.3 \text{ ms}$ $T_C = +25^{\circ}C$	R <sub>θJC</sub> (2) (4)	R <sub>θJC</sub> (3) (4)	$T_{STG}$ and $T_{J}$
	V dc	A dc	A (pk)	°C/W	°C/W	°C
1N7072CCT3	30	16A	150A	0.8	1.6	-65 to +150
1N7078U3	30	30A	150A	1.6	1.6	-65 to +150

- (1) See temperature-current derating curves on figures 3 and 4.
- (2) Entire package.
- (3) Each leg.
- (4) See thermal impedance curves on figures 5 and 6.
- 1.4 Primary electrical characteristics.  $R_{\theta JC} = 0.8^{\circ}\text{C/W}$  maximum entire package for 1N7072CCT3;  $R_{\theta JC} = 1.6^{\circ}\text{C/W}$  maximum entire package for 1N7078U3.

Comments, suggestions, or questions on this document should be addressed to DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to Semiconductor@dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at https://assist.dla.mil/.

AMSC N/A FSC 5961



- \* 1.5 Part or Identifying Number (PIN). The PIN is in accordance with MIL-PRF-19500, and as specified herein. See 6.5 for PIN construction example and 6.6 for a list of available PINs.
- \* 1.5.1 <u>JAN certification mark and quality level for encapsulated devices</u>. The quality level designators for encapsulated devices that are applicable for this specification sheet from the lowest to the highest level are as follows: "JAN", "JANTX", "JANTXV" and "JANS".
- \* 1.5.2 <u>Device type</u>. The designation system for the device types of diodes covered by this specification sheet are as follows.
- \* 1.5.2.1 <u>First number and first letter symbols</u>. The diodes of this specification sheet are identified by the first number and letter symbols "1N".
- \* 1.5.2.2 <u>Second number symbols</u>. The second number symbols for the diodes covered by this specification sheet are as follows: "7072CC" and "7078".
- \* 1.5.2.3 <u>Suffix letters</u>. The suffix letters "U3" are used on devices that are packaged in the surface mount package of figure 1. The suffix letters "T3" are used on devices that are packaged in the TO-257AA through hole package of figure 2.
- \* 1.5.3 Lead finish. The lead finishes applicable to this specification sheet are listed on QPDSIS-19500.

## 2. APPLICABLE DOCUMENTS

\* 2.1 <u>General</u>. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3 and 4 of this specification, whether or not they are listed.

## 2.2 Government documents.

2.2.1 <u>Specifications, standards, and handbooks</u>. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

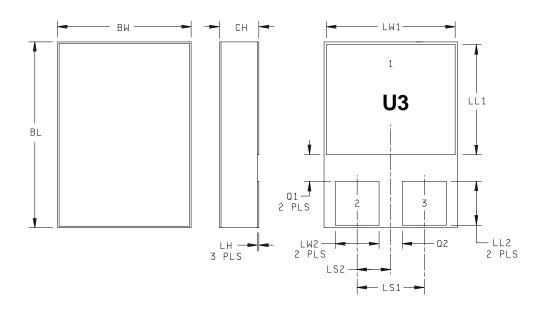
### DEPARTMENT OF DEFENSE SPECIFICATIONS

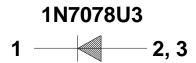
MIL-PRF-19500 - Semiconductor Devices, General Specification for.

# DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-750 - Test Methods for Semiconductor Devices.

- \* (Copies of these documents are available online at http://quicksearch.dla.mil/).
  - 2.3 <u>Order of precedence</u>. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

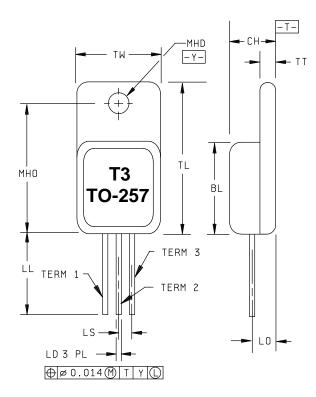




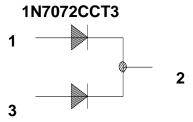
	Dimensions				
Ltr	Inc	hes	Millimeters		
	Min	Max	Min	Max	
BL	.395	.405	10.03	10.29	
BW	.291	.301	7.39	7.65	
CH	.108	.122	2.74	3.12	
LH	.010	.020	0.25	0.51	
LL1	.220	.230	5.59	5.84	
LL2	.115	.125	2.92	3.18	
LS1	.150	BSC	3.81	BSC	
LS2	.075	BSC	1.91	BSC	
LW1	.281	.291	7.14	7.39	
LW2	.090	.100	2.29	2.54	
Q1	.030		0.76		
Q2	.030		0.76		

- 1. Dimensions are in inches.
- 2. Millimeters are given for general information only.
- 3. Dimensions are in accordance with ASME Y14.5M, diameters are equivalent to  $\Phi x$  symbology.
- 4. Suffix "U3C" indicates a ceramic lid on package.

FIGURE 1. <u>Dimensions and configuration, 1N7078U3</u>.



		Dimer	nsions		
Ltr	Inc	hes	Millimeters		
	Min	Max	Min	Max	
BL	.410	.430	10.41	10.92	
CH	.190	.200	4.83	5.08	
LD	.025	.040	0.64	1.02	
LL	.500	.750	12.70	19.05	
LO	.120	BSC	3.05 BSC		
LS	.100	BSC	2.54 BSC		
MHD	.140	.150	3.56	3.81	
MHO	.527	.537	13.39	13.64	
TL	.645	.665	16.38	16.89	
TT	.035	.045	0.89	1.14	
TW	.410	.420	10.41	10.67	



- 1. Dimensions are in inches.
- 2. Millimeters are given for general information only.
- 3. In accordance with ASME Y14.5M, diameters are equivalent to  $\Phi x$  symbology.

FIGURE 2. Dimensions and configuration for 1N7072CCT3 (TO-257AA).

#### 3. REQUIREMENTS

- 3.1 General. The individual item requirements shall be as specified in MIL-PRF-19500 and as modified herein.
- 3.2 <u>Qualification</u>. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturer's list (QML) before contract award (see 4.2 and 6.3).
- 3.3 <u>Abbreviations, symbols, and definitions</u>. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500.
- 3.4 Interface and physical dimensions. The interface and physical dimensions shall be as specified in MIL-PRF-19500, and on figures 1 and 2 herein. Methods used for electrical isolation of the terminal feedthroughs for the TO-257 package shall employ materials that contain a minimum of 90 percent  $Al_2O_3$  (ceramic).
  - 3.4.1 Polarity. Polarity and terminal configuration shall be in accordance with figures 1 and 2 herein.
- 3.4.2 <u>Lead material, finish, and formation</u>. Lead material for the TO-257 package shall be Kovar, Alloy 52, or CuZr; a copper core or plated core is permitted. Lead finish shall be solderable in accordance with MIL-PRF-19500, MIL-STD-750, and herein. Where a choice of lead formation, material, or finish is desired, it shall be specified in the acquisition document (see 6.2). When lead formation is performed, as a minimum, the vendor shall perform 100 percent hermetic seal in accordance with screen 14 of table E-IV of MIL-PRF-19500 and 100 percent dc testing in accordance with table I, subgroup 2 herein.
- 3.5 <u>Electrical performance characteristics</u>. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.
  - 3.6 Electrical test requirements. The electrical test requirements shall be as specified in tables I and II herein.
  - 3.7 Marking. Marking shall be in accordance with MIL-PRF-19500 and herein.
- 3.8 <u>Workmanship</u>. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.
  - 4. VERIFICATION
  - 4.1 <u>Classification of inspections</u>. The inspection requirements specified herein are classified as follows:
    - a. Qualification inspection (see 4.2).
    - b. Screening (see 4.3).
    - c. Conformance inspection (see 4.4 and tables I and II herein).
- 4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500 and as specified herein.
- 4.2.1 <u>Group E qualification</u>. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table III tests, the tests specified in table III herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

4.3 <u>Screening (JANS, JANTXV, and JANTX levels)</u>. Screening shall be in accordance with table E-IV of <u>MIL-PRF-19500</u> and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (table E-IV of	Measurement				
MIL-PRF-19500)	JANS level	JANTX and JANTXV levels			
3b	Method 4066 of MIL-STD-750, condition A, one pulse, $t_p$ = 8.3 ms, $I_O$ = 0, $V_{RWM}$ = 0, $I_{FSM}$ = see 1.3 herein.	Method 4066 of MIL-STD-750, condition A, one pulse, $t_p = 8.3$ ms, $I_O = 0$ , $V_{RWM} = 0$ , $I_{FSM} = see 1.3$ herein.			
3c	Thermal impedance (see 4.3.2).	Thermal impedance (see 4.3.2).			
3d	Avalanche energy test (see 4.3.3).	Avalanche energy test (see 4.3.3).			
9, 10	Not applicable.	Not applicable.			
11	$V_{F1}$ and $I_{R1}$ .	$V_{F1}$ and $I_{R1}$ .			
12	See 4.3.1. 240 hours, minimum.	See 4.3.1. 48 hours minimum.			
13	Subgroups 2 and 3 of table I herein, $V_{F1}$ , $V_{F2}$ , $V_{F3}$ , and $I_{R1}$ ; $\Delta V_{F1} = \pm 50$ mV (pk); $\Delta V_{F2} = \pm 50$ mV (pk); $\Delta V_{F3} = \pm 50$ mV (pk); $\Delta I_{R1} = \pm 100$ percent from the initial value or $\pm 500$ uA, whichever is greater.	Subgroup 2 of table I herein; $V_{F1}$ , $V_{F2}$ , $V_{F3}$ , and $I_{R1}$ ; $\Delta V_{F1} = \pm 50$ mV (pk); $\Delta V_{F2} = \pm 50$ mV (pk); $\Delta V_{F3} = \pm 50$ mV (pk); $\Delta I_{R1} = \pm 100$ percent from the initial value or $\pm 500$ uA, whichever is greater.			

- 4.3.1 <u>High temperature reverse bias</u>. Reverse bias conditions are as follows: Method 1038 of MIL-STD-750, test condition A,  $V_R = 24 \text{ V dc}$ ;  $T_J = +100 ^{\circ}\text{C}$ .
- \* 4.3.2 <u>Thermal impedance</u>. The thermal impedance measurements shall be performed in accordance with method 3101 or 4081 of <u>MIL-STD-750</u> using the guidelines in that method for determining I<sub>M</sub>, I<sub>H</sub>, t<sub>H</sub>, and t<sub>MD</sub>. See table III, subgroup 4 and figures 5 and 6 herein.
  - 4.3.3 Avalanche energy test. The avalanche energy test is to be performed in accordance with method 4064 of MIL-STD-750 using the circuit as shown on figure 7 or equivalent. The Schottky rectifier under test must be capable of absorbing the reverse energy, as follows:  $I_{AS} = 1A$ ,  $V_{DF} = 30 \text{ V}$  minimum,  $L = 100 \mu\text{H}$ .
    - 4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500.
  - 4.4.1 <u>Group A inspection</u>. Group A inspection shall be conducted in accordance with table E-V of MIL-PRF-19500, and table I herein. Electrical measurements (end-points) and delta requirements shall be in accordance with the applicable steps of table II herein.

- 4.4.2 <u>Group B inspection</u>. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in tables E-VIA (JANS) and E-VIB (JAN, JANTX, and JANTXV) of MIL-PRF-19500 and as follows. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2, forward voltage test ( $V_{F1}$ ) and reverse leakage test ( $V_{F1}$ ) herein. Delta measurements shall be in accordance with table II herein.
- 4.4.2.1 Quality level JANS, table E-VIA of MIL-PRF-19500.

	<u>Subgroup</u>	Method	Condition
*	B4	1037	$\Delta T_C = +85^{\circ}C$ , $I_F = 2$ A minimum.
	B5	1038	Condition A, $V_R$ = 24 V dc, $T_J$ = +100°C, t = 340 hours min; heat sinking allowed. This test shall be extended to 1,000 hours for each wafer.
			As an alternative method a ten dice sample (or 1 die per wafer whichever is greater) from each individual wafer shall be qualified for 1,000 hours minimum, then each screened inspection lot requires 340 hours minimum when selected from qualified wafers.

4.4.2.2 Quality levels JAN, JANTX and JANTXV, table E-VIB of MIL-PRF-19500.

	<u>Subgroup</u>	<u>Method</u>	Condition
*	В3	1037	$\Delta T_C = +85^{\circ}C$ , $I_F = 2$ A minimum.

4.4.3 <u>Group C inspection</u>. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VII of MIL-PRF-19500. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2, forward voltage test  $(V_{F1})$  and reverse leakage test  $(I_{R1})$  herein. Delta measurements shall be in accordance with table II herein.

	Subgroup	Method	Condition
*	C2	2036	Condition A, weight = 10 lbs $(4.5 \text{ kg})$ , $t = 15 \text{ seconds}$ . Not applicable for U3 package.
	C5	4081	Limit for thermal resistance for 1N7072CCT3 is 1.6°C/W for each diode. Limit for thermal resistance for 1N7078U3 is 1.6°C/W for each diode.
*	C6	1037	$\Delta T_C = +85$ °C, $I_F = 2$ A minimum.
	C6	1038	Condition A, $V_R = 24 \text{ V}$ dc, $T_J = +100^{\circ}\text{C}$ , $t = 340$ hours minimum (for TX, TXV only); heat sinking allowed. This test shall be extended to 1,000 hours for each wafer. Separate samples may be used.
			As an alternative method a ten dice sample (or 1 die per wafer whichever is greater) from each individual wafer shall be qualified for 1,000 hours minimum, then each screened inspection lot requires 340 hours minimum when selected

- 4.4.4 <u>Group E inspection</u>. Group E inspection shall be conducted in accordance with the tests and conditions specified for subgroup testing in table E-IX of MIL-PRF-19500, and table III herein. Delta measurements shall be in accordance with table II herein.
  - 4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables as follows.

from qualified wafers.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

TABLE I. Group A inspection. 1/2/

la anostico		MIL-STD-750	O. marda ad	Lin	nits	1.134	
Inspection	Method	Conditions	Symbol	Min	Max	Unit	
Subgroup 1							
Visual and mechanical examination	2071						
Subgroup 2							
Thermal impedance 3/			$Z_{\theta JX}$			°C/W	
Forward voltage 1N7072 1N7078	4011	Condition B, pulsed test (see 4.5.1) $I_F = 7.5 \text{ A (pk)}$ $I_F = 15 \text{ A (pk)}$	V <sub>F1</sub>		0.48 0.51	V dc V dc	
Forward voltage 1N7072 1N7078	4011	Condition B, pulsed test (see 4.5.1) $I_F = 15 \text{ A (pk)}$ $I_F = 20 \text{ A (pk)}$	V <sub>F2</sub>		0.58 0.55	V dc V dc	
Forward voltage 1N7072 1N7078	4011	Condition B, pulsed test (see 4.5.1) $I_F = 16 \text{ A (pk)}$ $I_F = 30 \text{ A (pk)}$	V <sub>F3</sub>		0.60 0.62	V dc V dc	
Reverse current 1N7072 1N7078 Subgroup 3	4016	DC method $V_R = 30 \text{ V}$ $V_R = 30 \text{ V}$	I <sub>R1</sub>		1.0 1.0	mA dc mA dc	
High temperature operation:		T <sub>C</sub> = +125°C					
Forward voltage 1N7072 1N7078	4011	Condition B, pulsed test (see 4.5.1) $I_F = 7.5 \text{ A (pk)}$ $I_F = 15 \text{ A (pk)}$	$V_{F4}$		0.365 0.41	V dc V dc	
Forward voltage 1N7072 1N7078	4011	Condition B, pulsed test (see 4.5.1) $I_F = 15 \text{ A (pk)}$ $I_F = 20 \text{ A (pk)}$	V <sub>F5</sub>		0.52 0.47	V dc V dc	
Forward voltage 1N7072 1N7078	4011	Condition B, pulsed test (see 4.5.1) $I_F = 16 \text{ A (pk)}$ $I_F = 30 \text{ A (pk)}$	V <sub>F6</sub>		0.54 0.57	V dc V dc	
Reverse current 1N7072 1N7078	4016	DC method; $V_R = 30 \text{ V}$ $V_R = 30 \text{ V}$	I <sub>R2</sub>		270 270	mA dc mA dc	

See footnotes at end of table.

TABLE I. Group A inspection – Continued. 1/2/

la an antique		MIL-STD-750	0	Lin	nits	1.1
Inspection	Method	Conditions	Symbol	Min	Max	Unit
Low temperature operation:		$T_C = -55^{\circ}C$				
Forward voltage	4011	Condition B, pulsed test (see 4.5.1)	V <sub>F7</sub>			
1N7072 1N7078		$I_F = 7.5 \text{ A (pk)}$ $I_F = 15 \text{ A (pk)}$			0.57 0.58	V dc V dc
Forward voltage	4011	Condition B, pulsed test (see 4.5.1)	$V_{F8}$			
1N7072 1N7078	4044	$I_F = 15 \text{ A (pk)}$ $I_F = 20 \text{ A (pk)}$			0.65 0.61	V dc V dc
Forward voltage	4011	Condition B, pulsed test (see 4.5.1)	$V_{F9}$			
1N7072 1N7078		$I_F = 16 \text{ A (pk)}$ $I_F = 30 \text{ A (pk)}$			0.66 0.67	V dc V dc
Subgroup 4						
Junction capacitance	4001	$V_R = 5 \text{ V dc}, f = 1 \text{ MHz}, $ $V_{SIG} = 50 \text{ mV (p-p)}$	CJ			
1N7072 1N7078 <u>Subgroup 5</u>					2000 2000	pF pF
Not applicable						
Subgroup 6						
Surge	4066	Condition A, see 1.3, column 4 herein, ten surges each diode. 60 seconds between surges, (see 4.5.1)				
Electrical measurements		See table I, subgroup 2 herein				
Subgroup 7						
Dielectric withstanding voltage	1016	$V_R$ = 500 V dc; all leads shorted; measure from leads to case	DWV		10	μА
Scope display evaluation	4023	Stable only				
Electrical measurements		See table I, subgroup 2 herein				

<sup>1/</sup> For sampling plan, see MIL-PRF-19500.
2/ Each individual diode.
3/ This test required for the following end-point measurements only:
 Group B, subgroups 3 and 4 (JANS).
 Group B, subgroups 2 and 3 (JAN, JANTX, JANTXV).
 Group C, subgroups 2 and 6.

Group E, subgroup 1.

TABLE II. Groups B, C, and E delta requirements. 1/2/3/4/5/6/

Cton	Increation	M	IIL-STD-750	Cymhol	Lin	nits	Unit
Step	Inspection	Method	Conditions	Symbol	Min	Max	Unit
1.	Forward voltage 1N7072 1N7078	4011	Condition B $I_F = 7.5 \text{ A (pk)}$ $I_F = 15 \text{ A (pk)}$ pulsed (see 4.5.1)	ΔV <sub>F1</sub>	±50 mV dc from ir reading.		m initial
2.	Forward voltage  1N7072 1N7078	4011	Condition B $I_F = 15 \text{ A (pk)}$ $I_F = 20 \text{ A (pk)}$ pulsed (see 4.5.1)	$\Delta V_{F2}$	±50 m readir	nV dc fror ng.	m initial
3.	Forward voltage  1N7072 1N7078	4011	Condition B $I_F = 16 \text{ A (pk)}$ $I_F = 30 \text{ A (pk)}$ pulsed (see 4.5.1)	ΔV <sub>F3</sub>	±50 m readir	nV dc from	n initial
4.	Reverse current 1N7072 1N7078	4016	DC Method $V_R = 30V$ $V_R = 30V$	Δl <sub>R1</sub>	reading	ercent fro or ±500u ver is grea	ıΑ
5	Thermal impedance	3101	See 4.3.2	$Z_{\theta JX}$		-	

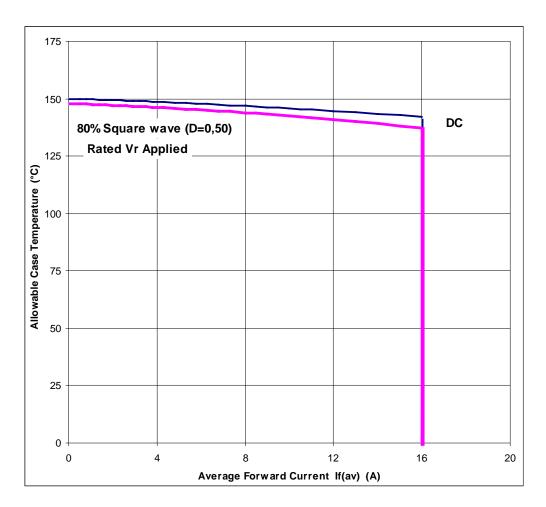
- 1/ Each individual diode.
- 2/ The delta measurements for table E-VIA (JANS) of MIL-PRF-19500 are as follows:
  - a. Subgroup 3, see table II herein, steps 1, 2, 3, 4, and 5.
  - b. Subgroup 4, see table II herein, steps 1, 2, 3, 4, and 5.
  - c. Subgroup 5, see table II herein, steps 1, 2, 3, and 4.
- \* 3/ The delta measurements for table E-VIB (JAN, JANTX and JANTXV) of MIL-PRF-19500 are as follows:
  - a. Subgroup 2, see table II herein, steps 1, 2, 3, 4, and 5.
  - b. Subgroup 3, see table II herein, steps 1, 2, 3, 4, and 5.
  - c. Subgroup 6, see table II herein, steps 1, 2, 3, and 4.
  - 4/ The delta measurements for table E-VII of MIL-PRF-19500 are as follows:
    - a. Subgroup 2, see table II herein, steps 1, 2, 3, 4, and 5 for all levels.
    - b. Subgroup 3, see table II herein, steps 1, 2, 3, and 4 for all levels.
    - c. Subgroup 6, see table II herein, steps 1, 2, 3, 4, and 5 for all levels.
  - 5/ The delta measurements for table E-IX of MIL-PRF-19500 are as follows:
    - a. Subgroup 1, see table III herein, steps 1, 2, 3, 4, and 5.
    - b. Subgroup 2, see table III herein, steps 1, 2, 3, and 4.
  - 6/ Devices which exceed the table I limits for this test shall not be accepted.

TABLE III. Group E inspection (all quality levels) – for qualification and requalification only.

Inspection	MIL-STD-750		Qualification	
mspection	Method	Conditions		
Subgroup 1			45 devices c = 0	
Temperature cycling (air to air)	1051	Test condition G, 500 cycles, -55°C to +150°C.		
Hermetic seal	1071			
Electrical measurements		See table I, subgroup 2 and table II herein.		
Subgroup 2			45 devices c = 0	
Life test	1048	$t = 1,000$ hours, $T_J = +100$ °C, $V_R = 80$ percent rated voltage (see 1.3, column 2 herein).	0 = 0	
Electrical measurements		See table I subgroup 2 and table II herein.		
Subgroup 4				
Thermal impedance curves		See MIL-PRF-19500.		
Subgroup 10 1/				
Surge	4066		5 devices c = 0	
1N7072		Condition A, $T_A = +25$ °C, $I_{FSM} = 150$ A, ten surges of 8.3 ms half sine wave. $V_R = 0$ ; $I_O = 10$ A pk.		
1N7078		Condition A, $T_A = +25$ °C, $I_{FSM} = 150$ A, ten surges of 8.3 ms half sine wave. $V_R = 0$ ; $I_O = 10$ A pk.		
Electrical measurements		See table I subgroup 2 ( $V_F$ and $I_R$ only).		

<sup>1/</sup> Each individual diode.

# TEMPERATURE-CURRENT DERATING CURVE 1N7072CCT3

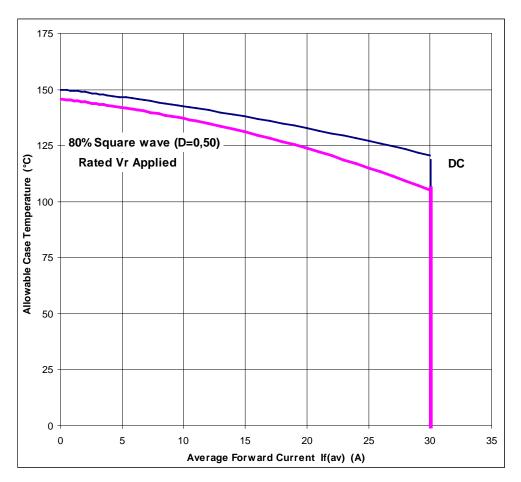


Switch mode operation, 80 percent duty cycle:  $T_C$  (°C) (case).  $R_{\theta,JC}$  = 0.8 °C/W.

- 1. All devices are capable of operating at ≤ T<sub>J</sub> specified on this curve. Any parallel line to this curve will intersect the appropriate current for the desired maximum T<sub>J</sub> allowed.
- 2. Derate design curve constrained by the maximum junction temperature ( $T_J \le 150^{\circ}C$ ) and current rating specified. (See 1.3 herein.)
- 3. Derate design curve chosen at  $T_J \le 125^{\circ}C$ , where the maximum temperature of electrical test is performed.
- 4. Derate design curves chosen at  $T_J \le 125^{\circ}C$ , and  $110^{\circ}C$  to show current rating where most users want to limit  $T_J$  in their application.

FIGURE 3. Temperature-current derating curve (entire package) for 1N7072CCT3.

# **TEMPERATURE-CURRENT DERATING CURVE** 1N7078U3



Switch mode operation, 80 percent duty cycle: T<sub>C</sub> (°C) (case).  $R_{\theta JC} = 1.6 \, ^{\circ}C/W$ .

- 1. All devices are capable of operating at  $\leq T_J$  specified on this curve. Any parallel line to this curve will intersect the appropriate current for the desired maximum T<sub>J</sub> allowed.
- 2. Derate design curve constrained by the maximum junction temperature (T<sub>J</sub> ≤ 150°C) and current rating specified. (See 1.3 herein.)
- 3. Derate design curve chosen at  $T_J \le 125^{\circ}C$ , where the maximum temperature of electrical test is performed. 4. Derate design curves chosen at  $T_J \le 125^{\circ}C$ , and  $110^{\circ}C$  to show current rating where most users want to limit  $T_J$ in their application.

FIGURE 4. Temperature-current derating curve (entire package) for 1N7078U3.

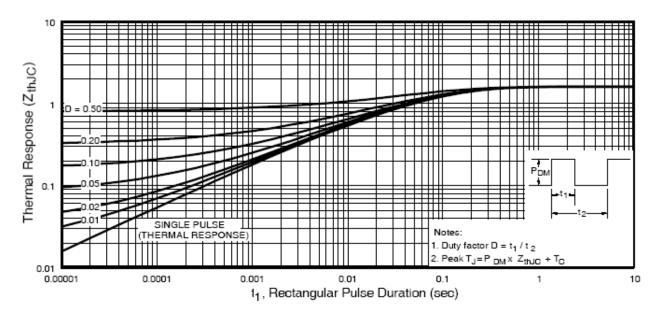


FIGURE 5. Thermal impedance (for each leg) 1N7072CCT3.

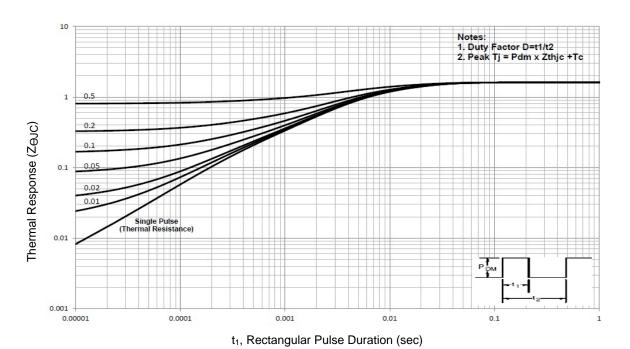
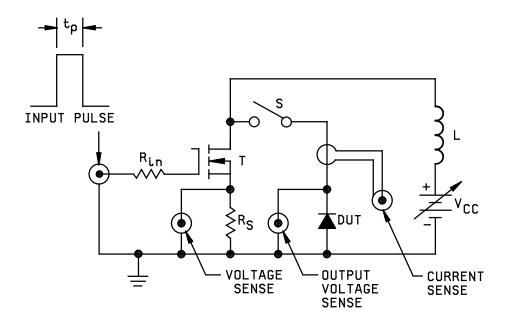


FIGURE 6. Thermal impedance 1N7078U3.



Input pulse  $R_{in}$  = 50 ohms  $V_G$  = 10 Volts,  $R_S$  = 0.1 ohms  $Z_G$  = 50 ohms L = 100 $\mu$ H Duty cycle  $\leq$  1 percent, T = IRF250/2N6766 or equivalent

# Procedure:

- 1. With S open, adjust pulse width to test current of 1 amp through  $R_{\mbox{\scriptsize S}}.$
- 2. Close S, verify test current with current sense.
- 3. Read peak output voltage (see 4.3.3).

FIGURE 7. Avalanche energy test circuit.

#### 5. PACKAGING

5.1 <u>Packaging</u>. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

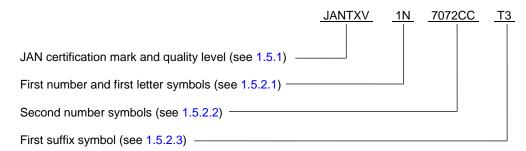
#### 6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in MIL-PRF-19500 are applicable to this specification.)

- 6.1 <u>Intended use</u>. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.
  - 6.2 Acquisition requirements. Acquisition documents should specify the following:
    - a. Title, number, and date of this specification.
    - b. Packaging requirements (see 5.1).
    - c. Lead material, finish, and formation (see 3.4.2).
- d. The complete PIN, see 1.5 and 6.6.1.
- 6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at https://assist.dla.mil.
- 6.4 <u>Cross reference substitution list</u>. A PIN for PIN replacement table follows, and these devices are directly interchangeable.

Non-preferred PIN	Preferred PIN
16SCYQ030C	JAN, JANTX, JANTXV, JANS1N7072CCT3
30SLJQ030	JAN, JANTX, JANTXV, JANS1N7078U3

- 6.5 <u>PIN construction example</u>.
- \* 6.5.1 Encapsulated devices The PINs for encapsulated devices are constructed using the following form.



- 6.6 <u>List of PINs</u>.
- \* 6.6.1 <u>List of PINs for encapsulated devices</u>. The following is a list of possible PINs for encapsulated devices available on this specification sheet.

PINs for devices of the base quality level	PINs for devices of the "TX" quality level	PINs for devices of the "TXV" quality level	PINs for devices of the "S" quality level
JAN1N7072CCT3	JANTX1N7072CCT3	JANTXV1N7072CCT3	JANS1N7072CCT3
JAN1N7078U3	JANTX1N7078U3	JANTXV1N7078U3	JANS1N7078U3

- \* 6.7 Request for new types and configurations. Requests for new device types or configurations for inclusions in this specification sheet should be submitted to: DLA Land and Maritime, ATTN: VAC, Post Office Box 3990, Columbus, OH 43218-3990 or by electronic mail at <a href="mailto:semiconductor@.dla.mil">Semiconductor@.dla.mil</a> or by facsimile (614) 693-1642 or DSN 850-6939.
- \* 6.8 Changes from previous issue. The margins of this specification are marked with asterisks to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodians:

Army - CR

Navy - EC

Air Force - 85

NASA - NA

DLA - CC

Review activities

Army - MI

Preparing activity:

(Project 5961-2016-032)

DLA - CC

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